

Serial No.: 10/041,848

action mentions 'Stephenson's sync detect' without citation to supporting text or drawings elements in the Stephenson reference. It is unclear as to precisely what 'sync detect' the office action is proposing to modify. Further, although the office action appears to utilize Stephenson as the primary reference, the purported motivation to modify the references is stated in terms of modifying Govindaraman with the teachings of Stephenson. If the rejection is maintained, clarification is respectfully requested.

In any event, the motivation as set forth is unworkable. The office action proposes to replace the Sync Detect block in Fig. 1 of Govindaraman with some functionally equivalent circuit from Stephenson. However, as explained in more detail in connection with Fig. 2, the Sync Detector 230 is part of a serial processing data path, including a serial processing NRZI decoder 240. The data isn't even converted to parallel format until later in the processing path at the serial to parallel converter 260. Accordingly, the 'sync detect' of Stephenson would not work in the circuit of Fig. 1 of Govindaraman. Moreover, the relied upon NRZI decoder 240 utilizes serial processing, not parallel data processing as recited in the claim.

Because the office action fails to establish motivation to combine the references, and because the proposed modification is unworkable, claim 1 is patentable over the combination of Stephenson and Govindaraman. Claims 2-6 depend either directly or indirectly from claim 1 and are likewise patentable.

The rejection of claim 5 is not understood because the language cited in the office action does not correspond to the claim language and the cited portion of the reference does not appear to read on the claim language. Clarification is respectfully requested.

With respect to claim 10, the office action completely fails to address the recitations of claim 10. Claim 10 is a method claim having a different scope as compared to claim 1. For example, the office completely fails to mention any recitations of claim 10 including at least: asserting a flag upon detection of the frame delineation marker; and creating a vector indicating a location of a frame boundary in the data stream. Applicants submit that neither of the cited references, alone or in combination, teach or suggest asserting a flag upon detection of the frame delineation marker; and creating a vector indicating a location of a frame boundary in the data stream. Accordingly, claim 10 and

Serial No.: 10/041,848

its dependent claims 11-16 are believed to be patentable. If the rejection is maintained, applicants are entitled to a new non-final action setting forth the Examiner's position with respect to claim 10.

With respect to claim 16, the claim recites that the vector created comprises an eleven-bit vector. Applicants note that the relied upon comparators 32 and 34 do not relate to the recited eleven-bit vector.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of U.S. Pat. No. 5,884,086 (Amoni). Applicants respectfully traverse this rejection for the following reasons.

Claim 7 recites one or more Universal Serial Bus (USB) connectors to couple to a communications channel carrying a USB data stream; an application specific integrated circuit comprising a USB transceiver, a serial interface engine and apparatus-specific logic, the USB transceiver having concurrent comparators to delineate received asynchronous frame boundaries within the USB data stream and parallel logic to decode received encoded data. The office action asserts, without support or citation to any text portion or drawings element, that Amoni discloses a USB transceiver, a serial interface engine, and apparatus specific logic. In fact, Amoni makes no reference to such elements. Accordingly, the office action fails to establish a prima facie case of obviousness. Amoni is related to providing power to USB 1.0 peripherals and does not discuss the transceiver / serial interface aspects of the USB devices.

In any event, the office action fails to establish proper motivation to combine the references. The office action proposes to modify Amoni with the teachings of Stephenson 'because this would have for the handling of high speed data streams in parallel.' Amoni, as noted above, is concerned with power delivery to USB 1.0 devices, and has no need for handling high speed data streams in parallel. As explicitly stated several times in Amoni, the top supported speed is 12 Mbits. In fact, Stephenson teaches away from the combination. Stephenson clearly states that the circuit disclosed therein is useful for data streams above 50 MHz (see col. 1, lines 27-34, col. 2, lines 32-40, and col. 5, line 66 - col. 6, line 3). Absent the hindsight afforded by the present specification,

Serial No.: 10/041,848

one of ordinary skill in the art would not be motivated to modify Amoni with the circuit of Stephenson because Stephenson's circuit is simply not necessary for handling a 12 Mbit data stream.

Moreover, the office action admits in connection with claim 1 that Stephenson fails to teach the recited parallel logic to decode received encoded data. The office action does not cite any portion of Amoni for this missing teaching.

Because the office action fails to establish a prima facie case of obviousness and because the office action fails to establish a proper motivation to combine the references, claim 7 is patentable over Stephenson in view of Amoni. Dependent claims 8 and 9 are likewise patentable.

Applicants note that claim 9 further recites that the parallel logic decodes non-return to zero invert (NRZI) encoded data, which was admitted as being absent from the teachings of Stephenson. Although Amoni mentions NRZI, Amoni does not teach or suggest parallel logic to decode NRZI encoded data.

Claims 12-13 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of Govindaraman and further in view of U.S. Pat. No. 6,041,430 (Yamauchi). Applicants respectfully traverse this rejection for the following reasons.

With respect to claims 12-13, these claims depend either directly or indirectly from patentable claim 10, and are also believed to be patentable. Yamauchi, which is relied upon for elements of claims 12 and 13, fails to make up for the deficiencies in the other references with respect to claim 10.

With respect to claim 17, for at least the reasons given above with respect to claim 1, the office action fails to establish motivation to combine Stephenson and Govindaraman, and further because the proposed modification is unworkable, claim 17 is patentable over the combination of Stephenson and Govindaraman. Claims 18-19 depend either directly or indirectly from claim 17 and are likewise patentable.

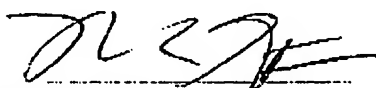
Serial No.: 10/041,848

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

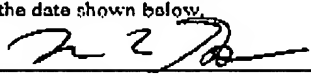
Respectfully submitted,

August 25, 2004

Date


Paul E. Steiner
Reg. No. 41,326
(703) 633 - 6830

Intel Americas
LF3
4030 Lafayette Center Drive
Chantilly, VA 20151

CERTIFICATE OF TRANSMISSION	
I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.	
By:  Paul E. Steiner	Date: 8/25/04